Chapter 3 & 4: Bipolar Junction Transistors and Applications
Transistor Construction

There are two types of transistors:

- \textit{pnp}
- \textit{nnp}

The terminals are labeled:

- \textit{E} - Emitter
- \textit{B} - Base
- \textit{C} - Collector
Transistor Operation

With the external sources, $V_{EE}$ and $V_{CC}$, connected as shown:

- The emitter-base junction is forward biased
- The base-collector junction is reverse biased
Currents in a Transistor

Emitter current is the sum of the collector and base currents:

\[ I_E = I_C + I_B \]

The collector current is comprised of two currents:

\[ I_C = I_{C_{\text{majority}}} + I_{C_{\text{minority}}} \]
Common-Base Configuration

The base is common to both input (emitter–base) and output (collector–base) of the transistor.
Common-Base Amplifier

Input Characteristics

This curve shows the relationship between of input current ($I_E$) to input voltage ($V_{BE}$) for three output voltage ($V_{CB}$) levels.
Common-Base Amplifier

Output Characteristics

This graph demonstrates the output current ($I_C$) to an output voltage ($V_{CB}$) for various levels of input current ($I_E$).

$$I_{CO} = I_{CBO}$$
Operating Regions

- **Active** – Operating range of the amplifier.
- **Cutoff** – The amplifier is basically off. There is voltage, but little current.
- **Saturation** – The amplifier is full on. There is current, but little voltage.

<table>
<thead>
<tr>
<th>Regions</th>
<th>Base-Emitter</th>
<th>Collector-Base</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active</td>
<td>Forward-biased</td>
<td>Reverse-biased</td>
</tr>
<tr>
<td>Cutoff</td>
<td>Reverse-biased</td>
<td>Reverse-biased</td>
</tr>
<tr>
<td>Saturation</td>
<td>Forward-biased</td>
<td>Forward-biased</td>
</tr>
</tbody>
</table>
Approximations

Emitter and collector currents:

\[ I_C \approx I_E \]

Base-emitter voltage:

\[ V_{BE} = 0.7 \text{ V (for Silicon)} \]
Alpha (α)

Alpha (α) is the ratio of $I_C$ to $I_E$:

$$\alpha_{dc} = \frac{I_C}{I_E}$$

Ideally: $\alpha = 1$
In reality: $\alpha$ is between 0.9 and 0.998

$IC = \alpha IE + ICBO$

Alpha (α) in the AC mode:

$$\alpha_{ac} = \left. \frac{\Delta I_C}{\Delta I_E} \right|_{V_{CB}} = \text{constant}$$
Transistor Amplification

Omit DC biasing to demonstrate AC response

Assume $R_i$ and $R_o$ from input & output characteristic curves

Currents and Voltages:

\[ I_E = I_i = \frac{V_i}{R_i} = \frac{200\text{mV}}{20\Omega} = 10\text{mA} \]

\[ I_C \approx I_E \]

\[ I_L \approx I_i = 10 \text{mA} \]

\[ V_L = I_L R = (10\text{mA})(5\text{k}\Omega) = 50 \text{V} \]

Voltage Gain:

\[ A_v = \frac{V_L}{V_i} = \frac{50\text{V}}{200\text{mV}} = 250 \]
Common–Emitter Configuration

The emitter is common to both input (base-emitter) and output (collector-emitter).

The input is on the base and the output is on the collector.
Common-Emitter Characteristics

Collector Characteristics

Base Characteristics
Common-Emitter Amplifier Currents

Ideal Currents

\[ I_E = I_C + I_B \quad \quad I_C = \alpha I_E \]

Actual Currents

\[ I_C = \alpha I_E + I_{CBO} \quad \text{where } I_{CBO} = \text{minority collector current} \]

\( I_{CBO} \) is usually so small that it can be ignored, except in high power transistors and in high temperature environments.

When \( I_B = 0 \mu A \) the transistor is in cutoff, but there is some minority current flowing called \( I_{CEO} \).

\[ I_{CEO} = \left. \frac{I_{CBO}}{1 - \alpha} \right|_{I_B=0 \mu A} \]
Beta ($\beta$)

$\beta$ represents the amplification factor of a transistor. ($\beta$ is sometimes referred to as $h_{fe}$, a term used in transistor modeling calculations)

In DC mode:

$$\beta_{dc} = \frac{I_C}{I_B}$$

In AC mode:

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B} \bigg|_{V_{CE}=\text{constant}}$$
Beta (β)

Determining β from a Graph

\[ \beta_{AC} = \frac{(3.2 \text{ mA} - 2.2 \text{ mA})}{(30 \mu\text{A} - 20 \mu\text{A})} \]
\[ = \frac{1 \text{ mA}}{10 \mu\text{A}} \bigg| V_{CE} = 7.5 \]
\[ = 100 \]

\[ \beta_{DC} = \frac{2.7 \text{ mA}}{25 \mu\text{A}} \bigg| V_{CE} = 7.5 \]
\[ = 108 \]

Both β values are usually reasonably close and are often used interchangeably.
Beta (β)

Relationship between amplification factors $\beta$ and $\alpha$

$$\alpha = \frac{\beta}{\beta + 1} \quad \beta = \frac{\alpha}{\alpha - 1}$$

Relationship Between Currents

$$I_C = \beta I_B \quad I_E = (\beta + 1) I_B$$
Common–Collector Configuration

The input is on the base and the output is on the emitter.
Common–Collector Configuration

The characteristics are similar to those of the common-emitter configuration, except the vertical axis is $I_E$. 

![Graph showing characteristics of the common-collector configuration](image-url)
Operating Limits for Each Configuration

$V_{CE}$ is at maximum and $I_C$ is at minimum ($I_{C\text{max}} = I_{CEO}$) in the cutoff region.

$I_C$ is at maximum and $V_{CE}$ is at minimum ($V_{CE\text{max}} = V_{CE\text{sat}} = V_{CEO}$) in the saturation region.

The transistor operates in the active region between saturation and cutoff.
Power Dissipation

Common-base:

\[ P_{C_{\text{max}}} = V_{CB} I_C \]

Common-emitter:

\[ P_{C_{\text{max}}} = V_{CE} I_C \]

Common-collector:

\[ P_{C_{\text{max}}} = V_{CE} I_E \]
Transistor Specification Sheet

### MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>2N4123</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector-Emitter Voltage</td>
<td>V_{CEO}</td>
<td>30</td>
<td>V dc</td>
</tr>
<tr>
<td>Collector-Base Voltage</td>
<td>V_{CEO}</td>
<td>40</td>
<td>V dc</td>
</tr>
<tr>
<td>Emitter-Base Voltage</td>
<td>V_{CEO}</td>
<td>5.0</td>
<td>V dc</td>
</tr>
<tr>
<td>Collector Current – Continuous</td>
<td>I_{C}</td>
<td>200</td>
<td>mA dc</td>
</tr>
<tr>
<td>Total Device Dissipation @ T_a = 25°C</td>
<td>P_o</td>
<td>625</td>
<td>mW</td>
</tr>
<tr>
<td>Derate above 25°C</td>
<td>P_o</td>
<td>5.0</td>
<td>mW/°C</td>
</tr>
<tr>
<td>Operating and Storage Junction Temperature Range</td>
<td>T_{J,MAX}</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

### THERMAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance, Junction to Case</td>
<td>R_{JC}</td>
<td>83.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance, Junction to Ambient</td>
<td>R_{JIA}</td>
<td>200</td>
<td>°C/W</td>
</tr>
</tbody>
</table>
Transistor Specification Sheet

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OFF CHARACTERISTICS</strong> (T_A = 25°C unless otherwise noted)**</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Collector-Emitter Breakdown Voltage (1)</td>
<td>V_BCEO</td>
<td>30</td>
<td></td>
<td>V_dc</td>
</tr>
<tr>
<td>(I_C = 1.0 mA dc, I_E = 0)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Collector-Base Breakdown Voltage</td>
<td>V_BCEO</td>
<td>40</td>
<td></td>
<td>V_dc</td>
</tr>
<tr>
<td>(I_C = 10 µA dc, I_E = 0)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Emitter-Base Breakdown Voltage</td>
<td>V_BREBO</td>
<td>5.0</td>
<td></td>
<td>V_dc</td>
</tr>
<tr>
<td>(I_E = 10 µA dc, I_C = 0)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Collector Cutoff Current (V_CE = 20 V dc, I_E = 0)</td>
<td>I_CRO</td>
<td></td>
<td>50</td>
<td>nA dc</td>
</tr>
<tr>
<td>Emitter Cutoff Current (V_BE = 5.0 V dc, I_C = 0)</td>
<td>I_EBO</td>
<td></td>
<td>50</td>
<td>nA dc</td>
</tr>
<tr>
<td><strong>ON CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC Current Gain (1)</td>
<td>h_FE</td>
<td>50</td>
<td>150</td>
<td>–</td>
</tr>
<tr>
<td>(I_C = 2.0 mA dc, V_CE = 1.0 V dc)</td>
<td></td>
<td>25</td>
<td></td>
<td>–</td>
</tr>
<tr>
<td>(I_C = 50 mA dc, V_CE = 1.0 V dc)</td>
<td></td>
<td></td>
<td></td>
<td>–</td>
</tr>
<tr>
<td>Collector-Emitter Saturation Voltage (1)</td>
<td>V_CE(on)</td>
<td>0.3</td>
<td></td>
<td>V_dc</td>
</tr>
<tr>
<td>(I_C = 50 mA dc, I_E = 5.0 mA dc)</td>
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<td></td>
<td></td>
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</tr>
<tr>
<td>Base-Emitter Saturation Voltage (1)</td>
<td>V_BE(on)</td>
<td>0.95</td>
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<td>V_dc</td>
</tr>
<tr>
<td>(I_C = 50 mA dc, I_E = 5.0 mA dc)</td>
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<tr>
<td><strong>SMALL-SIGNAL CHARACTERISTICS</strong></td>
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<tr>
<td>Current-Gain – Bandwidth Product</td>
<td>f_T</td>
<td>250</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>(I_C = 10 mA dc, V_CE = 20 V dc, f = 100 MHz)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Capacitance</td>
<td>C_BO</td>
<td>4.0</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>(V_CE = 5.0 V dc, I_E = 0, f = 100 MHz)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>C_BO</td>
<td>8.0</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>(V_BO = 0.5 V dc, I_C = 0, f = 100 kHz)</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Collector-Base Capacitance</td>
<td>C_B</td>
<td>4.0</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>(I_E = 0, V_CE = 5.0 V, f = 100 kHz)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Small-Signal Current Gain</td>
<td>h_FE</td>
<td>50</td>
<td>200</td>
<td>–</td>
</tr>
<tr>
<td>(I_C = 2.0 mA dc, V_CE = 10 V dc, f = 1.0 kHz)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Gain – High Frequency</td>
<td>h_FE</td>
<td>2.5</td>
<td>50</td>
<td>200</td>
</tr>
<tr>
<td>(I_C = 10 mA dc, V_CE = 20 V dc, f = 100 MHz)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_C = 2.0 mA dc, V_CE = 10 V, f = 1.0 kHz)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Noise Figure</td>
<td>NF</td>
<td>6.0</td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2.0%
Transistor Terminal Identification
Biasing: The DC voltages applied to a transistor in order to turn it on so that it can amplify the AC signal.

\[ V_{BE} = 0.7 \text{V} \]
\[ I_E = (\beta + 1)I_B \approx I_C \]
\[ I_C = \beta I_B \]
Operating Point

The DC input establishes an operating or quiescent point called the **Q-point**.
The Three States of Operation

• **Active or Linear Region Operation**
  Base–Emitter junction is forward biased
  Base–Collector junction is reverse biased

• **Cutoff Region Operation**
  Base–Emitter junction is reverse biased

• **Saturation Region Operation**
  Base–Emitter junction is forward biased
  Base–Collector junction is forward biased
DC Biasing Circuits

- Fixed-bias circuit
- Emitter-stabilized bias circuit
- Collector-emitter loop
- Voltage divider bias circuit
- DC bias with voltage feedback
Fixed Bias
The Base-Emitter Loop

From Kirchhoff’s voltage law:

\[ +V_{CC} - I_B R_B - V_{BE} = 0 \]

Solving for base current:

\[ I_B = \frac{V_{CC} - V_{BE}}{R_B} \]
Collector current:

\[ I_C = \beta I_B \]

From Kirchhoff’s voltage law:

\[ V_{CE} = V_{CC} - I_C R_C \]
Saturation

When the transistor is operating in saturation, current through the transistor is at its maximum possible value.

\[ I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C} \]

\[ V_{CE} \approx 0 \text{ V} \]

This approximation is equivalent to move the region below \( V_{CE_{\text{sat}}} \) of the output curves to align on the output current axis.
Load Line Analysis

The end points of the load line are:

- $I_{C_{sat}}$
  - $I_C = \frac{V_{CC}}{R_C}$
  - $V_{CE} = 0 \text{ V}$

- $V_{C_{E_{cutoff}}}$
  - $V_{CE} = V_{CC}$
  - $I_C = 0 \text{ mA}$

The $Q$-point is the operating point:

- where the value of $R_B$ sets the value of $I_B$
- that sets the values of $V_{CE}$ and $I_C$
Circuit Values Affect the Q-Point

more …
Circuit Values Affect the Q-Point

more …
Circuit Values Affect the Q-Point
Emitter-Stabilized Bias Circuit

Adding a resistor ($R_E$) to the emitter circuit stabilizes the bias circuit.
Base-Emitter Loop

From Kirchhoff’s voltage law:

\[ + V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \]

Since \( I_E = (\beta + 1)I_B \):

\[ V_{CC} - I_B R_B - V_{BE} - (\beta + 1)I_B R_E = 0 \]

Solving for \( I_B \):

\[ I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} \]
Collector-Emitter Loop

From Kirchhoff’s voltage law:

\[ I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0 \]

Since \( I_E \approx I_C \):

\[ V_{CE} = V_{CC} - I_C (R_C + R_E) \]

Also:

\[ V_E = I_E R_E \]
\[ V_C = V_{CE} + V_E = V_{CC} - I_C R_C \]
\[ V_B = V_{CC} - I_R R_B = V_{BE} + V_E \]
Improved Biased Stability

*Stability* refers to a circuit condition in which the currents and voltages will remain fairly constant over a wide range of temperatures and transistor Beta (β) values.

Adding $R_E$ to the emitter improves the stability of a transistor.

**Fixed-bias circuit**

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

**Emitter-stabilized bias circuit**

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$I_C = \beta I_B$$

$I_B$ in fixed-bias circuit cannot change, so change in $\beta$ results in large change in output current and voltage.
Saturation Level

The endpoints can be determined from the load line.

\[ V_{CE,\text{cutoff}}: \quad V_{CE} = V_{CC} \quad I_C = 0 \text{ mA} \]

\[ I_{C,\text{sat}}: \quad V_{CE} = 0 \text{ V} \quad I_C = \frac{V_{CC}}{R_C + R_E} \]
Voltage Divider Bias

This is a very stable bias circuit.

The currents and voltages are nearly independent of any variations in $\beta$. 
Approximate Analysis

Where $I_B << I_1$ and $I_1 \cong I_2$:

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Where $\beta R_E > 10R_2$:

$$I_E = \frac{V_E}{R_E}$$

$$V_E = V_B - V_{BE}$$

From Kirchhoff’s voltage law:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$I_E \cong I_C$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$
Voltage Divider Bias Analysis

Transistor Saturation Level

\[ I_{C_{\text{Sat}}} = I_{C_{\text{max}}} = \frac{V_{CC}}{R_C + R_E} \]

Load Line Analysis

Cutoff: Saturation:

\[ V_{CE} = V_{CC} \]
\[ I_C = 0 \text{mA} \]

\[ I_C = \frac{V_{CC}}{R_C + R_E} \]
\[ V_{CE} = 0 \text{V} \]
Voltage Divider Bias

\[ V_B = \left( \frac{R_2}{R_1 + R_2} \right) V_{cc} \]
\[ = \left( \frac{12 \text{ k}\Omega}{27 \text{ k}\Omega + 12 \text{ k}\Omega} \right)(+15 \text{ V}) = 4.62 \text{ V} \]

\[ V_E \text{ is one diode drop less than } V_B: \]
\[ V_E = 4.62 \text{ V} - 0.7 \text{ V} = 3.92 \text{ V} \]

Applying Ohm’s law:
\[ I_E = \frac{V_E}{R_E} = \frac{3.92 \text{ V}}{680 \Omega} = 5.76 \text{ mA} \]
Voltage Divider Bias (Exact)

\[ V_{TH} = V_{B\text{ (no load)}} = 4.62 \text{ V} \]

\[ R_{TH} = R_1 \parallel R_2 = 8.31 \text{ kΩ} \]

The Thevenin input circuit can be drawn.

\[ V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E \]

\[ I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}} \]

Substituting and solving,

\[ I_E = \frac{4.62 \text{ V} - 0.7 \text{ V}}{680 \text{ Ω} + 8.31 \text{ kΩ}/200} = 5.43 \text{ mA} \]

and \[ V_E = I_E R_E = (5.43 \text{ mA})(0.68 \text{ kΩ}) = 3.69 \text{ V} \]
Another way to improve the stability of a bias circuit is to add a feedback path from collector to base.

In this bias circuit the Q-point is only slightly dependent on the transistor beta, $\beta$. 
Base-Emitter Loop

From Kirchhoff’s voltage law:

$$V_{CC} - I'_{C} R_{C} - I_{B} R_{B} - V_{BE} - I_{E} R_{E} = 0$$

Where $I_{B} \ll I_{C}$:

$$I'_{C} = I_{C} + I_{B} \approx I_{C}$$

Knowing $I_{C} = \beta I_{B}$ and $I_{E} \approx I_{C}$, the loop equation becomes:

$$V_{CC} - \beta I_{B} R_{C} - I_{B} R_{B} - V_{BE} - \beta I_{B} R_{E} = 0$$

Solving for $I_{B}$:

$$I_{B} = \frac{V_{CC} - V_{BE}}{R_{B} + \beta(R_{C} + R_{E})}$$
Collector-Emitter Loop

Applying Kirchoff’s voltage law:

\[ I_E + V_{CE} + I'_C R_C - V_{CC} = 0 \]

Since \( I'_C \approx I_C \) and \( I_C = \beta I_B \):

\[ I_C(R_C + R_E) + V_{CE} - V_{CC} = 0 \]

Solving for \( V_{CE} \):

\[ V_{CE} = V_{CC} - I_C(R_C + R_E) \]
Base-Emitter Bias Analysis

Transistor Saturation Level

\[ I_{C_{\text{sat}}} = I_{C_{\text{max}}} = \frac{V_{CC}}{R_C + R_E} \]

Load Line Analysis

Cutoff:

\[ V_{CE} = V_{CC} \]
\[ I_C = 0 \text{ mA} \]

Saturation:

\[ I_C = \frac{V_{CC}}{R_C + R_E} \]
\[ V_{CE} = 0 \text{ V} \]
Transistor Switching Networks

Transistors with only the DC source applied can be used as electronic switches.
Switching Circuit Calculations

Saturation current:
\[ I_{\text{Csat}} = \frac{V_{\text{CC}}}{R_C} \]

To ensure saturation:
\[ I_B > \frac{I_{\text{Csat}}}{\beta_{\text{dc}}} \]

Emitter-collector resistance at saturation and cutoff:
\[ R_{\text{sat}} = \frac{V_{\text{CEsat}}}{I_{\text{Csat}}} \]
\[ R_{\text{cutoff}} = \frac{V_{\text{CC}}}{I_{\text{CEO}}} \]
Switching Time

Transistor switching times:

\[ t_{on} = t_r + t_d \]

\[ t_{off} = t_s + t_f \]
Troubleshooting Hints

• Approximate voltages
  – $V_{BE} \approx 0.7 \text{ V for silicon transistors}$
  – $V_{CE} \approx 25\% \text{ to } 75\% \text{ of } V_{CC}$
• Test for opens and shorts with an ohmmeter.
• Test the solder joints.
• Test the transistor with a transistor tester or a curve tracer.
• Note that the load or the next stage affects the transistor operation.
PNP Transistors

The analysis for \textit{pnp} transistor biasing circuits is the same as that for \textit{npn} transistor circuits. The only difference is that the currents are flowing in the opposite direction.
Homework 3 (Chapter 3)

- Common-Base Configuration
  - 3.4 (13)
- Transistor Amplifying Action
  - 3.5 (18)
- Common-Emitter Configuration
  - 3.6 (23)
Homework 3 (Chapter 4)

- Fixed-Bias Configuration
  - 4.3 (1)
- Emitter-Bias Configuration
  - 4.4 (8)
- Voltage Divider Configuration
  - 4.5 (13)
- Collector-Feedback Configuration
  - 4.6 (23)
- Miscellaneous Bias Configuration
  - 4.59 (30)